HIGH-EFFICIENCY BROADBAND POWER TRANSISTORS FOR S-BAND APPLICATIONS

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Abstract

A 50-ohm microwave power transistor has been developed for high-efficiency broadband applications at lower S-Band frequencies. The device is capable of providing 10 watts of output power with 9 dB gain and greater than 0.50 collector efficiency in a 50-ohm system.

Introduction

Initial development of an internally-matched S-Band microwave power transistor has been completed. Optimum performance is achieved when the device is operated directly in a 50-ohm system with no external circuitry other than that required for the DC bias voltage and the emitter ground return. This work was part of a program to develop an advanced integrated microwave transmitter which is capable of being used in a module as an element of a high power active array antenna.

Power Transistor Development

A complete family of transistors was designed to meet the requirements of the amplifier power chain. These characteristics are listed below.

Goals For S-Band Transistors

Characteristic	Stage First	Second	Third
Frequency band (GHz)	2.25-2.50	2.25-2.50	2.25-2.50
Gain (dB)	12.5 min	10.0 min	10.0 min
Output power (watts)	0.26 min	2.25 min	8.9 min
V_{cc} (volts)	20	20	20
Collector efficiency (percent)	60 min	60 min	60 min
Duty factor	0.4 max	0.4 max	0.4 max
Pulsewidth (μs)	25	25	25
Thermal impedance (°C/watt)	60 max	18 max	9 max
Junction temperature (°C)	120 max	120 max	120 max

This paper primarily presents the results of the third-stage power transistor development effort. At this level the high power and collector efficiency requirements dominate the overall effectiveness of the three stage amplifier.

Transistor Characterization

The silicon chip consists of four cells utilizing arsenic emitters and interdigitated geometry. Each cell has a 28.5 square mil base area and a 140.0 mil emitter periphery. The silicon chip is shown in Figure 1.

Characterization of the transistor chip for large-signal operation was performed through measurement of the required source and load impedances for one cell. One cell was mounted in the common base configuration and rf data was obtained in a test fixture. Output power and input match were maximized with variable slab-line screw tuners. Source and load impedances required to establish the operating condition were then documented. The parasitic contributions of the beryllia carrier were taken into account and the driving-point impedances required to conjugately match the device at the plane of the silicon chip were computed. These impedances were converted to admittances and multiplied by four to obtain the driving-point admittances to conjugately match a four-cell device. Measuring the impedances and correcting for header parasitics at the higher impedance levels of a single cell minimized the errors which are often introduced while characterizing low-impedance active devices. The impedances, obtained in the above manner, to conjugately match the four-cell device at the plane of the chip are:

$$Z_{Load} = 1.7 + j\ 5.9 \text{ ohms}$$

$$Z_{Source} = 0.64 + j\ 0.67 \text{ ohms}$$

Further characterization was completed in a similar manner over the frequency band of interest.

Bandwidth Restrictions

To properly utilize this transistor chip one would typically need to realize networks capable of a 75:1 impedance transformation on the input and a 30:1 transformation on the output. Minimal loss in these networks was a prime consideration since the required output power levels and collector efficiencies are considered to be state-of-the-art using available technology. Packaging the chip in a microwave header presents still another problem. The lumped equivalent circuit of a typical header is shown in Figure 2. Each parasitic element can be associated with necessary interconnections required to mount the silicon die and to feed its terminals to the package exterior. Mounting the chip in such a package would result in a significant increase in the input Q. This seriously degrades the device's broadband capability and represents the fundamental limitation in packaging microwave transistor chips for broadband power applications. The large-signal output impedance of the chip would be taken through series-resonance by the package parasitic inductance with a resulting output Q which is actually higher than that of the

transistor chip. No effective impedance transformation is realized through addition of this series reactance.

Chip Carrier Approach

This problem has been approached by incorporating into the basic header networks which result in complete impedance transformations to a 50-ohm level. This "chip carrier" approach represents a significant step forward in utilizing low-impedance devices, since it incorporates existing parasitics into a circuit design.

The chip carrier is illustrated in Figure 3. The device utilizes the four-cell arsenic emitter silicon chip and MOS chip capacitors alloyed directly to a beryllium oxide carrier. Beam lead capacitors and thin-film distributed elements printed on alumina form the upper level of the chip carrier. Wire bonding is used to interconnect the components on different levels. The complete device measures 0.40 x 0.40 x 0.70 inches and is configured to be compatible with microstrip circuitry. The circuit topology was optimized through the use of computer-aided design techniques and is depicted schematically in Figure 4. C_1, L_1, C_2, and L_2 represent equivalent reactances of wire bonds, MOS chip capacitors, and printed microstrip elements used to form an input network which transforms the device input impedance to 50-ohms over the frequency range of interest. L_3 represents the equivalent common-lead inductance of multiple base wires. L_4, L_5, C_4, and C_5 represent equivalent reactances of wire bonds and beam-lead capacitors. The shunt branches incorporating C_4, L_4, C_5, and L_5 are in parallel resonance with the device large-signal output capacitance and alloy pad capacitance, C_3. This parallel resonance at the silicon chip transforms the output impedance of the device to the range of 15 to 20 ohms while incurring negligible circuit losses. L_6 and C_6 complete the impedance transformation to a 50-ohm level and represent equivalent reactances of wire bonds and printed microstrip elements.

Chip Carrier Performance

Typical performance of the completed chip carrier in a 50-ohm system is shown in Figure 5. Transistor load sensitivity has also been characterized. Constant power contours (8, 9, 10, and 11 watts) and constant collector efficiency contours (0.50, 0.55, 0.60) are shown in Figure 6 and are useful in predicting performance when loaded with complex impedances other than 50-ohms.

The completed chip carrier was incorporated as the third-stage amplifier in the S-Band multistage amplifier shown in Figure 7. Typical performance of this prototype amplifier is shown for several duty factor conditions in Figure 8.

Conclusion

Current MIC technology has been applied to develop a broadband microwave transistor chip carrier for pulsed or continuous duty at S-Band frequencies.

Acknowledgements

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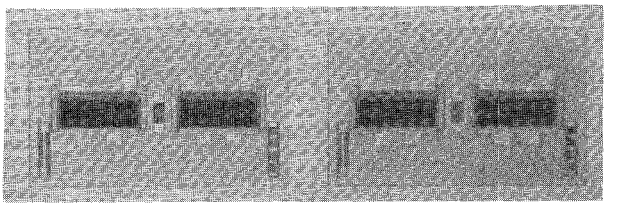

Fig. 1 Silicon chip, 4-cell

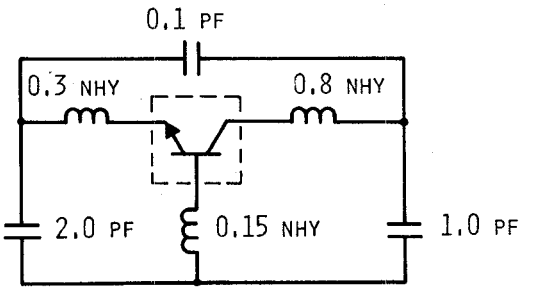

Fig. 2 Typical microwave header, lumped equivalent circuit

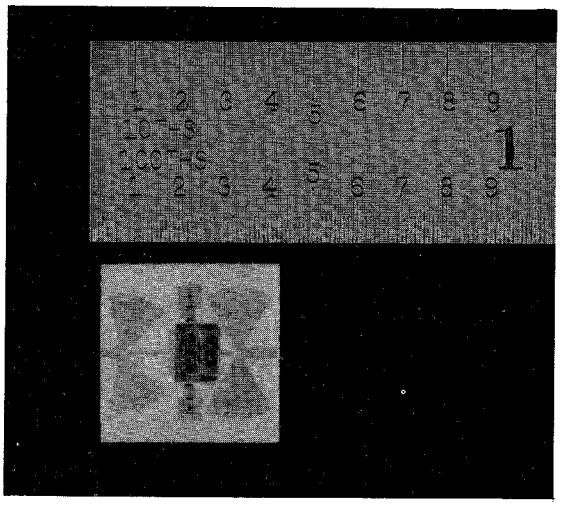

Fig. 3 S-Band chip carrier

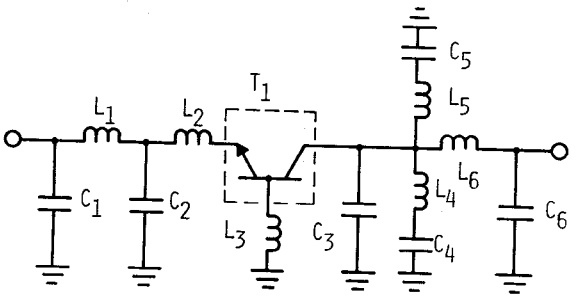

Fig. 4 Schematic, S-Band chip carrier

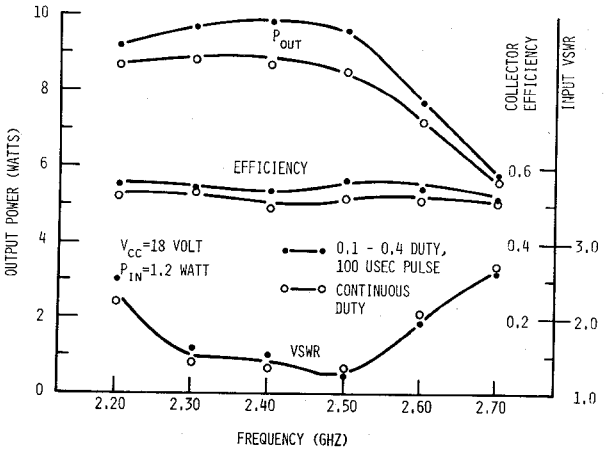

Fig. 5 Typical performance, S-Band chip carrier

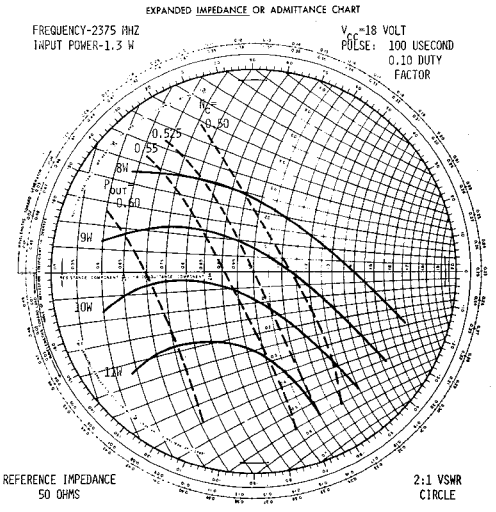

Fig. 6 Load and efficiency contours, 2375 MHz

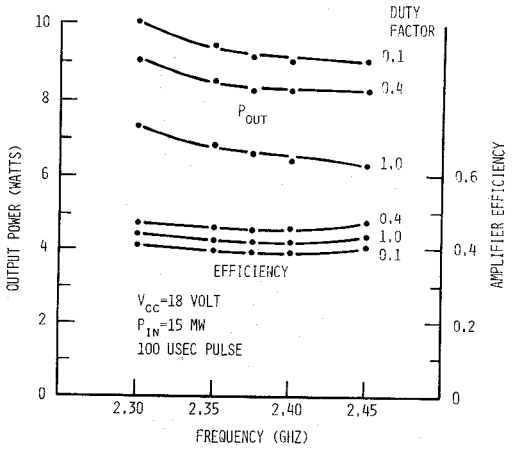

Fig. 8 Prototype amplifier performance

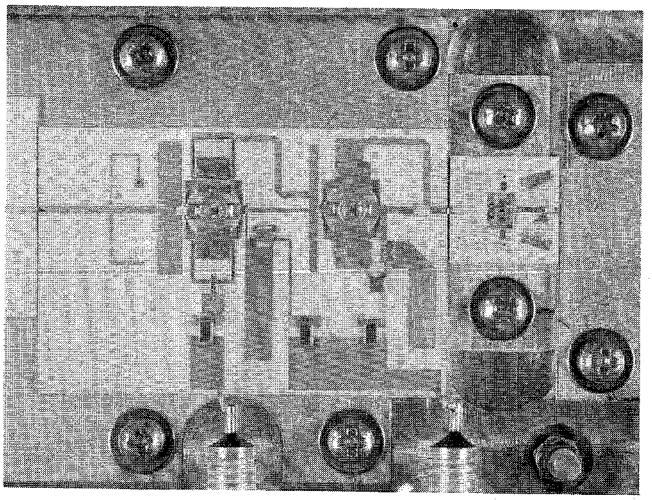

Fig. 7 S-Band multistage amplifier